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10/516,843	12/03/2004	Jan Hoogerbrugge	NL02 0480 US	7262

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EXAMINER	
AYASH, MARWAN	
ART UNIT	**PAPER NUMBER**
2185	

SHORTENED STATUTORY PERIOD OF RESPONSE	MAIL DATE	DELIVERY MODE
3 MONTHS	03/08/2007	PAPER

Please find below and/or attached an Office communication concerning this application or proceeding.

If NO period for reply is specified above, the maximum statutory period will apply and will expire 6 MONTHS from the mailing date of this communication.

Office Action Summary	Application No.	Applicant(s)	
	10/516,843	HOOGERBRUGGE ET AL.	
	Examiner	Art Unit	
	Marwan Ayash	2185	

-- The MAILING DATE of this communication appears on the cover sheet with the correspondence address --

Period for Reply

A SHORTENED STATUTORY PERIOD FOR REPLY IS SET TO EXPIRE 3 MONTH(S) OR THIRTY (30) DAYS, WHICHEVER IS LONGER, FROM THE MAILING DATE OF THIS COMMUNICATION.

- Extensions of time may be available under the provisions of 37 CFR 1.136(a). In no event, however, may a reply be timely filed after SIX (6) MONTHS from the mailing date of this communication.
- If NO period for reply is specified above, the maximum statutory period will apply and will expire SIX (6) MONTHS from the mailing date of this communication.
- Failure to reply within the set or extended period for reply will, by statute, cause the application to become ABANDONED (35 U.S.C. § 133). Any reply received by the Office later than three months after the mailing date of this communication, even if timely filed, may reduce any earned patent term adjustment. See 37 CFR 1.704(b).

Status

1)☒ Responsive to communication(s) filed on *23 January 2007*.

2a)☒ This action is **FINAL**. 2b)☐ This action is non-final.

3)☐ Since this application is in condition for allowance except for formal matters, prosecution as to the merits is closed in accordance with the practice under *Ex parte Quayle*, 1935 C.D. 11, 453 O.G. 213.

Disposition of Claims

4)☒ Claim(s) *1-23* is/are pending in the application.

4a) Of the above claim(s) _____ is/are withdrawn from consideration.

5)☐ Claim(s) _____ is/are allowed.

6)☒ Claim(s) *1-23* is/are rejected.

7)☐ Claim(s) _____ is/are objected to.

8)☐ Claim(s) _____ are subject to restriction and/or election requirement.

Application Papers

9)☐ The specification is objected to by the Examiner.

10)☐ The drawing(s) filed on _____ is/are: a)☐ accepted or b)☐ objected to by the Examiner.

Applicant may not request that any objection to the drawing(s) be held in abeyance. See 37 CFR 1.85(a).

Replacement drawing sheet(s) including the correction is required if the drawing(s) is objected to. See 37 CFR 1.121(d).

11)☐ The oath or declaration is objected to by the Examiner. Note the attached Office Action or form PTO-152.

Priority under 35 U.S.C. § 119

12)☐ Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).

a)☐ All b)☐ Some * c)☐ None of:

1.☐ Certified copies of the priority documents have been received.

2.☐ Certified copies of the priority documents have been received in Application No. _____.

3.☐ Copies of the certified copies of the priority documents have been received in this National Stage application from the International Bureau (PCT Rule 17.2(a)).

* See the attached detailed Office action for a list of the certified copies not received.

Attachment(s)

1) ☒ Notice of References Cited (PTO-892)
2) ☐ Notice of Draftsperson's Patent Drawing Review (PTO-948)
3) ☐ Information Disclosure Statement(s) (PTO/SB/08) Paper No(s)/Mail Date _____.
4) ☐ Interview Summary (PTO-413) Paper No(s)/Mail Date. _____.
5) ☐ Notice of Informal Patent Application
6) ☐ Other: _____.

DETAILED ACTION

Response to Amendment

This office action has been issued in response to the amendment filed 1/23/07. Claims 1-23 are pending, claim 24 has been cancelled. Applicant's arguments have been carefully considered, but are not persuasive in view of the prior art. In addition, new grounds for rejection have been necessitated by amendments to the claims. Accordingly this action has been made FINAL.

Double Patenting

1. The nonstatutory double patenting rejection is based on a judicially created doctrine grounded in public policy (a policy reflected in the statute) so as to prevent the unjustified or improper timewise extension of the "right to exclude" granted by a patent and to prevent possible harassment by multiple assignees. A nonstatutory obviousness-type double patenting rejection is appropriate where the conflicting claims are not identical, but at least one examined application claim is not patentably distinct from the reference claim(s) because the examined application claim is either anticipated by, or would have been obvious over, the reference claim(s). See, e.g., *In re Berg*, 140 F.3d 1428, 46 USPQ2d 1226 (Fed. Cir. 1998); *In re Goodman*, 11 F.3d 1046, 29 USPQ2d 2010 (Fed. Cir. 1993); *In re Longi*, 759 F.2d 887, 225 USPQ 645 (Fed. Cir. 1985); *In re Van Ornum*, 686 F.2d 937, 214 USPQ 761 (CCPA 1982); *In re Vogel*, 422 F.2d 438, 164 USPQ 619 (CCPA 1970); and *In re Thorington*, 418 F.2d 528, 163 USPQ 644 (CCPA 1969).

A timely filed terminal disclaimer in compliance with 37 CFR 1.321(c) or 1.321(d) may be used to overcome an actual or provisional rejection based on a nonstatutory double patenting ground provided the conflicting application or patent either is shown to be commonly owned with this application, or claims an invention made as a result of activities undertaken within the scope of a joint research agreement.

Effective January 1, 1994, a registered attorney or agent of record may sign a terminal disclaimer. A terminal disclaimer signed by the assignee must fully comply with 37 CFR 3.73(b).

2. Claims 1, 7, 10,12, 18, 21 are provisionally rejected under the judicially created doctrine of obviousness-type double patenting as being unpatentable over claims 9,1, 3, 10, 4, 6 respectively of copending Application No. 10/495403. Although the conflicting claims are not identical, they are not patentably distinct from each other (see table below).

This is a provisional obviousness-type double patenting rejection because the conflicting claims have not in fact been patented.

As instant claims 1, 7, 10, 12, 18, 21 and copending claims 9,1, 3, 10, 4, 6 respectively, anticipate each other as detailed below, and as anticipation is the epitome of obviousness, no Graham v. Deere factors are necessary in this instance.

A later patent claim is not patentably distinct from an earlier patent claim if the later claim is obvious over, or anticipated by, the earlier claim. In re Longi, 759 F.2d at 896, 225 USPQ at 651 (affirming a holding of obviousness-type double patenting because the claims at issue were obvious over claims in four prior art patents); In re Berg, 140 F.3d at 1437, 46 USPQ2d at 1233 (Fed. Cir. 1998) (Affirming a holding of obviousness type double patenting where a patent application claim to a genus is anticipated by a patent claim to a species within that genus). " ELI LILLY AND COMPANY v BARR LABORATORIES, INC., United States Court of Appeals for the Federal Circuit, ON PETITION FOR REHEARING EN BANC (DECIDED: May 30, 2001).

The following table indicates the interpretation of examiner.

Instant application 10/516843	**10/495403 --- Co-pending application**
1. Device for writing data elements from a coprocessor into a FIFO memory, in a multiprocessing environment comprising at least one coprocessor, a FIFO memory and a controller, said device comprising:	**9.** Device for writing data elements into a shared FIFO buffer (100) on the basis of semaphore operations, comprising:
first counter for counting the available room in said FIFO memory;	first determining means (14) for determining if storage space (room) is available in said FIFO buffer (100) to store data elements therein;
second counter for counting the number of data elements written into said FIFO memory;	write counter (12) for incrementing the count thereof when data elements are input in step c), said count indicating the number of the data elements input in said FIFO buffer (100);

control means for checking said first counter for available room in said FIFO memory, for checking said second counter whether a predetermined number N of data elements have been written into said FIFO memory, for decrementing the count of said first counter and for incrementing the count of said second counter after a data element has been written into said FIFO memory;	first determining means (14) for determining if storage space (room) is available in said FIFO buffer (100) to store data elements therein; write counter (12) for incrementing the count thereof when data elements are input in step c), said count indicating the number of the data elements input in said FIFO buffer (100);
output means for outputting data elements to said FIFO memory;	input means (11) for inputting data elements into said FIFO buffer (100), -- [in both claims data is being written to the FIFO buffer]
wherein said control means is adapted to issue a first message when the count of said second counter has reached said predetermined number N by incrementing of the count of said second counter after a data element has been written into said FIFO memory; wherein said control means is adapted to issue a first call for available room in said FIFO memory to said controller; and wherein said output means is adapted to forward said first message and/or said first call to said controller.	first signalling means (13) for performing a first signalling operation when said count of said writer counter (12) has been incremented by L.

7. Method for writing data elements from a coprocessor into a FIFO memory being in a multiprocessing environment comprising at least one coprocessor, a FIFO memory and a controller, said method comprising the steps of:	1.Method for writing data elements into a shared FIFO buffer (100) on the basis of semaphore operations, comprising the steps of:
checking a first counter, indicating the available room in said FIFO memory, in order to determine whether there is room available in said FIFO memory	determining if storage space (room) is available in said FIFO buffer (100) to store data elements therein;

issuing a first call for available room in said FIFO memory to said controller until there is room in said FIFO memory; outputting data elements to said FIFO memory;	b) blocking the input of said FIFO buffer (100) if it has been determined in step a) that no storage space (room) is available in said FIFO buffer (100); c) inputting data elements into said FIFO buffer (100), if it has been determined in step a) that storage space (room) is available in said FIFO buffer (100);
decrementing the count of said first counter after a data element has been written into said FIFO memory; incrementing a second counter for counting the number of data elements written into said FIFO memory after a data element has been written into said FIFO memory;	d) incrementing the count of a write counter (12), when a data element is input in step c), said count indicating the number of the data elements input in said FIFO buffer (100);
checking said second counter in order to determine whether a predetermined number N of data elements have been written into said FIFO memory; and issuing a first message that sufficient data elements have been written into said FIFO memory when the count of said second counter has reached said predetermined number N by incrementing of the count of said second counter after a data element has been written into said FIFO memory.	e) performing a first signalling operation when said count of said writer counter (12) has been incremented by L.

10. Method according to claim 7, further comprising to step of: resetting said second counter after issuing said first message.	**3.** Method according to claim 1, wherein said step d) comprises the step of incrementing said count of said write counter (12) from a predefined starting count; said method further comprising the steps of: f) determining whether said count of said write counter (12) has reached a predefined first limit L, g) resetting said count of said write counter (12) to said predefined starting point after step f).

Claim 12 (symmetric to claim 1) only reading instead of writing	**Claim 10 symmetric to clam 9 only reading instead of writing - and since these claims are symmetric, they are rejected using the same reasoning.**

18. Method for reading data elements from a FIFO memory into a coprocessor being in a multiprocessing environment comprising at least one coprocessor, a FIFO memory and a controller, said method comprising the steps of:	**4.** Method for reading data elements from a shared FIFO buffer (100) on the basis of semaphore operations, comprising the steps of:
checking a third counter, indicating the available data elements in said FIFO memory, in order to determine whether there is data element available in said FIFO memory, issuing a second call for available data elements in said FIFO memory to said controller until there is data element in said FIFO memory; inputting data elements from said FIFO memory;	determining if data elements are available in said FIFO buffer (100) to be read from said FIFO buffer (100); b) blocking the output of said FIFO buffer (100) if it has been determined in step a) that no data elements are available in said FIFO buffer (100) to be read from said FIFO buffer (100); c) outputting data elements from said FIFO buffer (100), if it has been determined in step a) that data elements are available in said FIFO buffer (100) to be read from said FIFO buffer (100);
decrementing the count of said third counter after a data element has been read from said FIFO memory; incrementing a fourth counter for counting the number of data elements read from said FIFO memory after a data element has been read from said FIFO memory;	d) incrementing the count of a reader counter (22), when a data element is output from said FIFO buffer (100) in step c), said count indicating the number of the data elements output from said FIFO buffer (100);
checking said fourth counter in order to determine whether a predetermined number N of data elements have been read from said FIFO memory; and issuing a second message that sufficient data elements have been read from said FIFO memory when the count of said fourth counter has reached said predetermined number N by incrementing of the count of said second counter after a data element has been written into said FIFO memory;	e) performing a second signalling operation when said count of said read counter (17) has been incremented by L.

21. Method according to claim 18, further comprising to step of: resetting said fourth counter after issuing said second message.	**6.** Method according to claim 4, wherein said step d) further comprises the step of incrementing said count of said read counter (17) from a predefined starting count; said method further comprising the steps of: f) determining whether said count of said read counter (12) has reached a predefined first limit L, g) resetting said count of said read counter (12) to said predefined starting point after step f).

Claim Rejections - 35 USC § 102

3. The following is a quotation of the appropriate paragraphs of 35 U.S.C. 102 that form the basis for the rejections under this section made in this Office action:

> A person shall be entitled to a patent unless –
>
> (b) the invention was patented or described in a printed publication in this or a foreign country or in public use or on sale in this country, more than one year prior to the date of application for patent in the United States.

4. **Claims 1,7,12,18 are rejected** under 35 U.S.C. 102(e) as being anticipated by Robertson (US Patent # 6,892,253).

With respect to **independent claims 1,7, 12, 18** Robertson discloses a device (fig. 4) for writing data elements from a coprocessor into a FIFO memory, in a multiprocessing environment comprising at least one coprocessor, a FIFO memory and a controller, said device comprising:

-- a first counter (251) for counting the available room in said FIFO memory [see abstract];

-- a second counter (252) for counting the number of data elements written into said FIFO memory [see abstract];

-- control means for checking said first counter for available room in said FIFO memory, for checking said second counter whether a predetermined number N of data elements have been written into said FIFO

memory, for decrementing the count of said first counter and for incrementing the count of said second counter after a data element has been written into said FIFO memory [see abstract]; and

-- output means for outputting data elements to said FIFO memory [see fig. 4, the pipeline stages output data to the FIFO buffer 410];

-- wherein said control means is adapted to issue a first message when the count of said second counter has reached said predetermined number N by incrementing of the count of said second counter after a data element has been written into said FIFO memory [*the remote count 252 (second counter) is incremented upon allocation of data to the FIFO (Robertson - abstract) and decremented upon deallocation of data from FIFO; a FIFO has an output signal that indicates when it has passed some threshold of fullness (i.e. has reached a predetermined number - being incremented to that predetermined number), and this is used to prevent the FIFO from overflowing (Robertson – Col 5 lines 7-20); thus it is clear that Robertson discloses control means adapted to issue a first message (signal) when the count of the second counter, which tracks how much data has been input into the FIFO has reached a predetermined number; see also exemplary implementation of a full flag as a means of preventing FIFO overflow described in Col 5 lines 21-60 of Robertson*];

-- wherein said control means is adapted to issue a first call for available room in said FIFO memory to said controller [Column 7 lines 64-67]; and

-- wherein said output means is adapted to forward said first message and/or said first call to said controller [Column 7 lines 64-67].

Claim Rejections - 35 USC § 103

5. The following is a quotation of 35 U.S.C. 103(a) which forms the basis for all obviousness rejections set forth in this Office action:

(a) A patent may not be obtained though the invention is not identically disclosed or described as set forth in section 102 of this title, if the differences between the subject matter sought to be patented and the prior art are such that the subject matter as a whole would have been obvious at the time the invention was made to a person having ordinary skill in the art to which said subject matter pertains. Patentability shall not be negatived by the manner in which the invention was made.

6. The factual inquiries set forth in *Graham* **v.** *John Deere Co.*, 383 U.S. 1, 148 USPQ 459 (1966), that are applied for establishing a background for determining obviousness under 35 U.S.C. 103(a) are summarized as follows:

1. Determining the scope and contents of the prior art.
2. Ascertaining the differences between the prior art and the claims at issue.
3. Resolving the level of ordinary skill in the pertinent art.
4. Considering objective evidence present in the application indicating obviousness or nonobviousness.

7. **Claims 1-23 are rejected** under 35 U.S.C. 103(a) as being unpatentable over Bender et al. (US Patent # 5,664,223) in view of Robertson (US Patent # 6,892,253).

With respect to **independent claims 1, 7, 12, 18** Bender discloses a Device (& method) for writing (& reading) data elements from a coprocessor into a FIFO memory, in a multiprocessing environment [*an adaptor for transferring data between a main processor and its memory and a packet switch* (Bender - Column 2 lines 39-41)] comprising at least one coprocessor [*a communication processor* (Bender - Column 2 line 46), later referred to as a communication coprocessor (Bender - Column 2 line 65) and as a microprocessor 22 (Bender - Column 10 lines 13-14)], a FIFO memory [*bidirectional (bidi) first-in-first-out (FIFO) buffer* (Bender - Column 2 lines 42-43)] and a controller [*DRAM controller* (Bender - Column 5 line 19)]. Note that Bender's disclosure concerning the adapter for transferring data between a main processor and its memory and a packet switch is a high level summary of his invention which encompasses a coprocessor writing data elements into a FIFO memory.

-- control means for checking said first counter for available room in said FIFO memory [*determine if there is space in the outgoing FIFO* (Bender - Column 11 lines 2-6)], for checking said second counter whether a predetermined number N of data elements have been written into said FIFO memory [*checks to see if the tail*

pointer (+2) is not equal to the header pointer (Bender - Column 11 lines 2-6) – comparison between tail pointer and head pointer could just as likely be between predetermined number N and head pointer], And although "decrementing the count of said first counter and incrementing the count of said second counter after a data element has been written into said FIFO memory" is not explicitly disclosed, Bender teaches [*When data is put into the FIFO, the tail pointer is incremented and when data is taken out of the FIFO the head pointer is incremented* (Bender - Column 10 lines 40-43). Also see (Bender - Column 8 lines 51-67, here, two counters are implemented to keep track of read/write requests in FIFO memory). Note that the head and tail pointers are implemented inter alia to keep track of the amount of data in the FIFO queue - very much like the two counters of the instant application.]

-- output means for outputting data elements to said FIFO memory; disclosed as: [*send and receive operations using the bidi FIFO may be performed concurrently* (Bender - Column 13 lines 31-32), and as: *allows the adaptor to know which FIFO to put the data in* (Bender - Column 11 lines 36-37), and as: *If there is space in the outgoing FIFO, the main processor 2 will write the packet into the FIFO* (Bender - Column 11 lines 6-8)].

-- wherein said control means is adapted to issue a first message [*inform the coprocessor by putting a message into its memory*] when the count of said second counter has reached said predetermined number N [comparison of pointers in Bender's disclosure is interpreted to be functionally identical to checking if second counter has reached a predetermined value]; disclosed as: [*checks to see if the tail pointer (+2) is not equal to the header pointer*] (Bender - Column 11 lines 4-6), and as: [*main processor on the outgoing side will move the packet into its outgoing FIFO and will inform the coprocessor by putting a message into its memory*] (Bender - Column 10 lines 16-18).

-- wherein said control means is adapted to issue a first call for available room [*If it is full, local polling occurs at the coprocessor*] in said FIFO memory to said controller and wherein said output means is adapted

to forward said first message and/or said first call to said controller [*polling*]; disclosed as: [*If it is full, local polling occurs at the coprocessor. While there is polling occurring, the main processor can send a new "receive head" through the adaptor to thereby update the "receive head" in the coprocessor 22*] (Bender - Column 13 lines 10-14). Note that a memory and switch management unit 27 (MSMU) includes a plurality of registers and is operatively coupled to the microprocessor 22, the bidi FIFO, the HPS, and the DRAM 23 and serves as the DRAM controller (Bender - See figure 2).

Bender does not explicitly disclose a first counter for counting the available room in said FIFO memory and a second counter for counting the number of data elements written into said FIFO memory - although his invention implements two counters, $DMA_{pending}$ *and* DMA_{reply} to keep track of read/write requests in FIFO memory (Bender - Column 8 line 46 - Column 9 line 3), in addition to a head and tail pointer for indicating the amount of data in the FIFO queue (Bender - Column 10 lines 58-64).

Robertson teaches the use of two counters: A master count 251 indicating the number of entries available for use within the FIFO, and a remote count 252 indicating the number of data entries stored in the FIFO (Robertson - Abstract).

Bender and Robertson are analogous art because they are from the same field of endeavor of computer memory access (I/O) and control.

Therefore Bender in view of Robertson disclose all limitations of the instant claim including:

-- wherein said control means is adapted to issue a first message when the count of said second counter has reached said predetermined number N by incrementing of the count of said second counter after a data element has been written into said FIFO memory [*the remote count 252 (second counter) is incremented upon allocation of data to the FIFO (Robertson - abstract) and decremented upon deallocation of data from FIFO; a FIFO has an output signal that indicates when it has passed some threshold of fullness (i.e. has reached a predetermined number - being incremented to that predetermined number), and this is used to*

prevent the FIFO from overflowing (Robertson – Col 5 lines 7-20); thus it is clear that Robertson discloses control means adapted to issue a first message (signal) when the count of the second counter, which tracks how much data has been input into the FIFO has reached a predetermined number; see also exemplary implementation of a full flag as a means of preventing FIFO overflow described in Col 5 lines 21-60 of Robertson];

It would have been obvious to one having ordinary skill in the art at the time the invention was made to employ two counters as a means of capacity indication in the device of Bender as taught by Robertson because this would allow Bender to provide his invention with the capability to make better use of available bandwidth (Robertson - Abstract).

With respect to independent claims 12, 18 Bender's invention is capable of performing the steps of the claimed method and includes all elements of the claimed device since reading and writing are symmetric operations as is well known by the applicant (paragraph [0006] of applicant's specification).

With respect to **dependent claim 2, 13** as applied to claim 1, 12 above, Device according to claim 1, wherein said first message indicates that sufficient data elements have been written into said FIFO memory disclosed as: main processor on the outgoing side will move the packet into its outgoing FIFO and will inform the coprocessor by putting a message into its memory (Bender - Column 10 lines 16-18).

With respect to **dependent claims 3, 8, 14, 19** as applied to claims 2, 7, 13, 18 above, Device according to claim 2, wherein said control means is further adapted to increment a write pointer, when data elements were output to said FIFO memory. disclosed as: When data is put into the FIFO, the tail pointer is incremented and when data is taken out of the FIFO the head pointer is incremented (Bender - Column 10 lines 39-42).

With respect to **dependent claims 4, 9, 15, 20** as applied to claims 3, 8, 14, 19 above, Device according to claim 3, wherein said control means is further adapted to perform a wrap-around test after said

write pointer was incremented disclosed as: checks to see if the tail pointer (+2) is not equal to the header pointer (Bender - Column 11 lines 4-6).

With respect to **dependent claims 5, 10, 16, 21** as applied to claims 2, 7, 13, 18 above, Device according to claim 2, wherein said control means is adapted to reset said second counter after issuing said first message disclosed as: a reset device, operatively coupled to said output of the counting mechanism, for resetting the adaptor; and a reset transmitting device, operatively coupled between the reset device and the main processor for transmitting the reset condition of the adaptor to the main processor (Bender - Column 3 lines 35-40).

With respect to **dependent claims 6, 11, 17, 22** as applied to claims 1, 7, 13, 18 above, Device according to claim 1, wherein said control means is adapted to issue said first call for available room in said FIFO memory to said controller before said count of said first counter becomes zero disclosed as: it first polls the head pointer in its local memory and compares it with its cached value of the tail pointer to determine if there is space in the outgoing FIFO... checks to see if the tail pointer (+2) is not equal to the header pointer (Bender - Column 11 lines 2-6), and as: If it is full, local polling occurs at the coprocessor. While there is polling ~~is~~ occurring, the main processor can send a new "receive head" through the adaptor to thereby update the "receive head" in the coprocessor 22. (Bender - Column 13 lines 10-14). Note that issuing the call before the count of first counter becomes zero is the same as setting a predetermined threshold value which indicates an almost full state for the FIFO queue and issuing the call based on the counter or pointer reaching that value.

With respect to **claim 23,** Bender discloses a Multiprocessing computer system, comprising: a FIFO memory; at least one coprocessor; a controller, a device for writing according to claim 1 - (See rejection of claim 1 above).

Response to Arguments

1. Applicant's arguments filed 1/23/07 have been fully considered but they are not persuasive. The rejection of claims 1-23 is maintained, and clarification/elaboration on how/why the claims are not in condition for allowance will hereafter be provided (and made distinct via italicizing) in order to efficiently further prosecution.

1ST ARGUMENT:

With respect to applicants' argument on page 9 and that: The combination of the following features is not taught or suggested by Robertson: A feature of the invention as presently claimed is a second counter [*remote count 252 (Robertson – abstract, Col 5 lines 48-63)*] for counting the number of data elements written into a FIFO memory. When the second counter has reached a predetermined number N [*some threshold in terms of fullness (Robertson – Col 5 lines 7-20)*], control means issues a first message [*output signal issued upon reaching above mentioned threshold (Robertson – Col 5 line 11)*]. Output means forwards the first message to a controller [(*Robertson – Col 5 lines 64-67*)].

It is the examiners understanding that the alleged deficiencies of the prior art have now been addressed and clarified.

Conclusion

When responding to the office action, applicants are advised to clearly point out the patentable novelty which they think the claims present in view of the state of the art disclosed by the references cited or the objections made. Applicants must also show how the amendments avoid such references or objections. See 37 C.F.R. 1.111(c). In addition, applicants are advised to provide the examiner with the line numbers and page numbers in the application and/or references cited to assist examiner in locating the appropriate paragraphs.

THIS ACTION IS MADE FINAL. Applicant is reminded of the extension of time policy as set forth in 37 CFR 1.136(a).

A shortened statutory period for reply to this final action is set to expire THREE MONTHS from the mailing date of this action. In the event a first reply is filed within TWO MONTHS of the mailing date of this final action and the advisory action is not mailed until after the end of the THREE-MONTH shortened statutory period, then the shortened statutory period will expire on the date the advisory action is mailed, and any extension fee pursuant to 37 CFR 1.136(a) will be calculated from the mailing date of the advisory action. In no event, however, will the statutory period for reply expire later than SIX MONTHS from the mailing date of this final action.

Any inquiry concerning this communication or earlier communications from the examiner should be directed to Marwan Ayash whose telephone number is 571-270-1179. The examiner can normally be reached on Mon-Fri 9am-6pm.

If attempts to reach the examiner by telephone are unsuccessful, the examiner's supervisor, Sanjiv Shah can be reached on (571)272-4098. The fax phone number for the organization where this application or proceeding is assigned is 571-273-8300.

Information regarding the status of an application may be obtained from the Patent Application Information Retrieval (PAIR) system. Status information for published applications may be obtained from either Private PAIR or Public PAIR. Status information for unpublished applications is available through Private PAIR only. For more information about the PAIR system, see http://pair-direct.uspto.gov. Should you have questions on access to the Private PAIR system, contact the Electronic Business Center (EBC) at 866-217-9197 (toll-free). If you would like assistance from a USPTO Customer Service Representative or access to the automated information system, call 800-786-9199 (IN USA OR CANADA) or 571-272-1000.

Marwan Ayash
Examiner
Art Unit 2185

2/28/07

SANJIV SHAH
SUPERVISORY PATENT EXAMINER
TECHNOLOGY CENTER 2100